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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,968	02/25/2004	Christopher M. Mayer	A0312.70524US00	4111

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EXAMINER	
JOHNSON, BRIAN P	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/786,968	MAYER, CHRISTOPHER M.	
	Examiner	Art Unit	
	Brian P. Johnson	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1-12 have been examined.

Acknowledgment of papers filed: amendments and remarks filed on 9 September 2006. The papers filed have been placed on record.

Specification

2. The title is accepted. Objection is withdrawn.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

The claimed invention as a whole must be useful and accomplish a practical application. That is, it must produce a "useful, concrete and tangible result." State Street, 149 F.3d at 1373-74, 47 USPQ2d at 1601-02.

The tangible requirement does not necessarily mean that a claim must either be tied to a particular machine or apparatus or must operate to change articles or materials to a different state or thing. However, the tangible requirement does require that the claim must recite more than a Sec. 101 judicial exception, in that the process claim must set forth a practical application of that Sec. 101 judicial exception to produce a real-world result. Benson, 409 U.S. at 71-72, 175 USPQ at 676-77 (invention ineligible because had "no substantial practical application."). "[A]n application of a law of nature

or mathematical formula to a . . . process may well be deserving of patent protection." Diehr, 450 U.S. at 187, 209 USPQ at 8 (emphasis added); see also Corning, 56 U.S. (15 How.) at 268, 14 L.Ed. 683 ("It is for the discovery or invention of some practical method or means of producing a beneficial result or effect, that a patent is granted . . ."). In other words, the opposite meaning of "tangible" is "abstract."

In particular, claims 1-12, the claimed invention does not have a tangible result.

As per claims 1, 6 and 9, the final step is no more than a determination of whether or not the next instruction is a loop bottom instruction. There is no tangible result.

As per the remaining claims, each gives a more limited description of how the method/apparatus makes this determination, but gives no indication of a tangible result subsequent to the determination.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2, 5, 6, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue (Publication No. 2002/0078333) in view of Applicant's background.

Regarding claim 1, Inoue discloses a method for processing instructions in a pipelined processor (P10), comprising: decoding instructions to identify a loop setup instruction (P19) having a loop setup instruction address (see below)

Note that the loop setup instruction is fetched from addressable memory so, clearly, the instruction as an instruction address.

And containing a loop bottom offset (P26); decoding instructions following the loop setup instruction, each having an instruction address and containing an instruction width (see below);

Note that, clearly, these subsequent instructions from the addressable memory have both a width and an address.

And for each instruction following the loop setup instruction, using a current instruction address, a current instruction width, the loop setup instruction address and the loop bottom offset to determine if the next instruction is a loop bottom instruction (P26, P30, P39).

Inoue fails to disclose that the instructions used are variable-width.

Applicant's specification discloses the use of variable-width instructions (page 2 lines 11-16).

Examiner asserts that one of ordinary skill in the art realizes the advantage of variable-width instructions. Variable-width instructions allows the programmer to more effectively utilize memory and hardware area by limiting the length of instructions that do not require extra bits, saving area, power, and cost in many cases. Inoue, an instruction that already takes into account the width of an instruction for loop execution

calculations, would be motivated to incorporate variable length instructions for those reasons.

It would have been obvious at the time of the invention for one of ordinary skill in the art to allow the invention of Inoue to incorporate variable length instructions, as those disclosed in Applicant's background.

Note that this combination is applicable to all remaining claims. For the sake of simplicity, the combination will be known herein as Inoue.

6. Regarding claim 2, Inoue discloses a method as defined in claim 1, wherein determining if the next instruction is a loop bottom instruction comprises determining if the current instruction address plus the current instruction width minus the loop setup instruction address minus the loop bottom offset is equal to zero (P39, P19 and P26).

Note that the disclosed citation is logically equivalent to the claimed formula. P39 discloses calculating the loop top instruction by adding the width from the offset. The second citation, P19, states that a "bottom match" is requirement, suggesting a comparison between the PC value and the loop bottom address. This comparator (as known by those of skill in the art) is logically equivalent to a subtraction between the current instruction value (added to the width) and the loop bottom address and comparing the result to zero. Additionally, the loop bottom instruction is calculated based on the address of the setup instruction and the loop bottom offset (P26). If all this logic is factored in, the claimed formula is found to be logically equivalent.

7. Regarding claim 5, Inoue discloses a method as defined in claim 1, further comprising identifying a next instruction following the loop setup instruction as a loop bottom instruction if the loop bottom offset is equal to a width of the loop setup instruction (P39).

8. Regarding claim 6, Inoue discloses apparatus for processing variable width instructions (see claim 1) in a pipeline processor, comprising: an instruction decoder configured to decode a loop setup instruction (P19), having a loop setup instruction address (see claim 1), to obtain a loop bottom offset and configured to decode instructions following the loop setup instruction, each having an instruction address (see claim 1), to obtain an instruction width; registers for holding the loop setup instruction address and the loop bottom offset (P26); and a loop bottom detector (P19), responsive to a current instruction address (P19), a current instruction width (P39), the loop setup instruction address and the loop bottom offset (P26), configured to determine if a next instruction is a loop bottom instruction (P19).

9. Regarding claim 9, Inoue discloses apparatus for processing variable width instructions (see claim 1) in a pipelined processor (P10), comprising: means for decoding a loop setup instruction (P19), having a loop setup instruction address (see claim 1), to obtain a loop bottom offset and for decoding instructions following the loop setup instruction, each having an instruction address (P26), to obtain an instruction width (P39); means for holding the loop setup instruction address and the loop bottom

offset (P26); and means, responsive to a current instruction address (P19), a current instruction width (P39), the loop setup instruction address and the loop bottom offset (P26), for determining if a next instruction is a loop bottom instruction (P19).

10. Regarding claim 10, Inoue discloses apparatus as defined in claim 9, wherein the means for determining if a next instruction is a loop bottom instruction comprises means for determining if the current instruction address plus the current instruction width minus the loop setup instruction address minus the loop bottom offset is equal to zero.

Note: see claim 2.

Allowable Subject Matter

11. Claims 3, 4, 7, 8, 11 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and rewritten to overcome the rejection under 35 USC 101, without adding any further limitations requiring consideration.

Regarding claims 3, 7, and 11, no prior art on record discloses determining whether or not a next instruction is a loop bottom instruction using the formula given, in addition to all other limitations of the claims.

Regarding claims 4, 8, and 12, they are dependant on claims 3, 7, and 11 respectively.

Response to Arguments

12. Applicant's arguments filed 08 September 2006 have been fully considered but they are not persuasive.

13. Applicant states:

"the present claims are not even remotely of the type that merit crutiny under 35 U.S.C. 101. Indeed, the present claims easily pass the even stricter 'technology arts' test previously applied by the Patent Office which was overturned by the courts as an unlawful restriction of 35 U.S.C. 101."

Examiner disagrees. 35 USC 101 requires a useful, tangible result. The patent office has recently interpreted this to require the final step of each method claim, or apparatus claim with method step equivalent language, to be concluded with a tangible result. In the instruction processing art, this is interpreted to require a "state change" for the processing system. In particular, a register or memory of some sort must be altered within the claim. For example, regarding claim 1, determining if the next instruction is a loop bottom instruction, by itself, requires no state change and is not a tangible result. If Applicant amended the claims in a way to show that this determined result was stored or used in some fashion that required a state change, then the rejection would be withdrawn."

14. Applicant states:

"The rejection based on Sing is improper...under the American Intventers Protection Act of 1999"

Examiner agrees. A new grounds rejection is presented with a reference that has been published on June 20th, 2002.

Conclusion

The following is text cited from 37 CFR 1.11(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RICHARD L. ELLIS
RIMARY EXAMINER